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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
FREDERICK N. HAUSE
JEFFREY C. HAINES
MICHAEL E. EXTERKAMP

Serial No.: 10/023,347

Filed: December 17, 2001

For: METHOD OF FORMING AN ALIGNMENT MARK ON A WAFER, AND A WAFER COMPRISING SAME

Examiner: L. Schillinger

Group Art Unit: 2813

Att'y Docket: 2000.031300

Customer NO. 023720

APPEAL BRIEF

CERTIFICATE OF MAILING
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11.18.05 (Date) Kathy Klaras (Signature)

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final Office Action dated July 25, 2005. A Notice of Appeal was filed on September 30, 2005 and so this Appeal Brief is believed to be timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500) from **Advanced Micro Devices, Inc.'s Deposit Account 01-0365/TT3618.**[1]

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[1] In the event the monies in that account are insufficient, the Director is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.031300.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc. The assignment of the present application to Advanced Micro Devices, Inc., is recorded at Reel 12406, Frame 0955.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-12 are pending in the application. Claims 1-2, 4-8, and 10-12 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Nishihara, et al (U.S. Patent No. 5,286,673). Claim 3 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nishihara in view of Ridinger (U.S. Patent No. 4,724,219). Claim 9 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Nishihara in view of Jang (U.S. Patent No. 6,049,137).

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 sets forth providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting layer positioned above the insulating layer. For example, Applicants describe forming a silicon-on-insulator

(SOI) structure including a silicon substrate, a silicon dioxide insulating layer, and an epitaxial silicon semiconductor layer. See Patent Application, page 10, ll. 21-24 and Figure 1.

Independent claim 1 also sets forth forming an opening in the semiconducting layer and the insulating layer to thereby expose a surface area of the bulk substrate, and forming an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate. For example, one or more etching processes may be performed to define an opening 20 in a semiconducting layer 16 and an insulating layer 14. The opening 20 defines an exposed area 24 of the bulk substrate 12 wherein the surface 22 of the bulk substrate 12 is exposed for further processing. An alignment mark 30 (see Figure 4) may be formed in the bulk substrate 12 in the exposed area 24 of the bulk substrate 12 within the opening 20. See Patent Application, page 11, ll. 14-20 and Figure 3. In one embodiment, a patterned layer of photoresist 26 may be used as a mask to form the alignment mark 30 in the bulk substrate 12. After formation of the patterned photoresist layer 26, one or more etching processes are performed to define the alignment mark 30 in the bulk substrate 12 within the exposed area 24 defined by the opening 20. See Patent Application, page 12, ll. 5-11 and Figure 4.

Independent claim 1 further sets forth forming a layer of material above the alignment mark and in the opening. For example, a layer of material 32 may be formed in the opening 20 and above the alignment mark 30 formed in the bulk substrate 12. The layer 32 may be comprised of a variety of insulating and/or non-insulating materials. In one embodiment, the layer 32 may be comprised of silicon dioxide, silicon oxynitride, silicon nitride, or any other material having a dielectric constant less than approximately 8. Moreover, the layer of material 32 may be formed as a separate process step to cover the alignment mark 30, or it may be formed as part of another process, *e.g.*, a silicon dioxide fill of previously formed shallow trench

isolation regions (not shown) in the semiconducting layer 16. See Patent Application, page 12, line 23 – page 13, line 6 and Figure 6.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully requests that the Board review and overturn the three rejections present in this case. The following issues are presented on appeal in this case:

(A) Whether claims 1-2, 4-8, and 10-12 are anticipated by Nishihara;

(B) Whether claim 3 is obvious over Nishihara in view of Ridinger; and

(C) Whether claim 9 is obvious over Nishihara in view of Jang.

VII. ARGUMENT

A. Legal Standards

An anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Inherency in anticipation requires that the asserted proposition *necessarily* flow from the disclosure. *In re Oelrich*, 212 U.S.P.Q. (BNA) 323, 326 (C.C.P.A. 1981); *Levy*, 17 U.S.P.Q.2d (BNA) at 1463-64; *Skinner*, at 1789; *In re King*, 231 U.S.P.Q. (BNA) 136, 138 (Fed. Cir. 1986). It is not enough that a reference could have, should have, or would have been used as the claimed invention. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Oelrich*, at 326, quoting *Hansgirg v. Kemmer*, 40 U.S.P.Q. (BNA) 665, 667 (C.C.P.A. 1939); *In re Rijckaert*, 28 U.S.P.Q.2d (BNA) 1955, 1957 (Fed. Cir. 1993), quoting *Oelrich*, at 326; *see also Skinner*, at 1789.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. Moreover, it is the claimed invention, as a whole, that must be considered for purposes of determining obviousness. A mere selection of various bits and pieces of the claimed invention from various sources of prior art

does not render a claimed invention obvious, unless there is a suggestion or motivation in the prior art for the claimed invention, when considered as a whole.

It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine,* 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

B. Claims 1-2, 4-8, and 10-12 are not anticipated by Nishihara.

Nishihara describes forming a silicon dioxide layer 2 over a silicon substrate 1 and forming an opening 9a in the silicon dioxide layer 2. See Nishihara, col. 4, ll. 5-10 and Figure 5(a). A conductive poly-silicon film is deposited over the entire surface of the silicon substrate 1 and then the conductive poly-silicon film is etched using a photoresist mask 7 to form an alignment marking electrode 3a in the opening 9a in the silicon dioxide layer 2. See Nishihara, col. 4, ll. 11-20 and Figure 5(b). In rejecting independent claim 1, the Examiner has apparently equated the silicon substrate 1 with the bulk substrate, the silicon dioxide layer 2 with the insulating layer, and the conductive poly-silicon film with the silicon semiconductor layer. Applicants respectfully submit that equating these layers is incorrect because the poly-silicon film described in Nishihara is conductive and therefore is not a semiconductor layer.

In response to the above argument, the Examiner alleges that a person of ordinary skill in the art would know that a polysilicon material may be used as a semiconductor. Applicants respectfully submit that whether or not the polysilicon material may or may not be used as a semiconductor is irrelevant to determining whether the present invention is anticipated by Nishihara because Nishihara has explicitly stated that the polysilicon film deposited over the

entire surface of the silicon substrate 1 is conductive. Accordingly, Applicants maintain that the conductive polysilicon film described in Nishihara is not a semiconductor layer and Nishihara therefore fails to teach or suggest, explicitly or inherently, providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting layer positioned above the insulating layer.

Even if the Examiner's reasoning is accepted for the sake of argument, Nishihara still fails to describe or suggest all the limitations of independent claim 1. As discussed above, Nishihara describes forming an opening 9a in the silicon dioxide layer 2 and depositing the conductive poly-silicon layer over the entire surface of the silicon substrate 1. Nishihara then describes etching the conductive poly-silicon film using a photoresist mask 7 to form an alignment marking electrode 3a in the opening 9a. Applying the Examiner's (erroneous) equations of the silicon substrate 1 with the bulk substrate, the silicon dioxide layer 2 with the insulating layer, and the conductive poly-silicon film with the silicon semiconductor layer, the description in Nishihara would correspond to forming an opening in the insulating layer, depositing the silicon semiconductor layer over the insulating layer, and etching the silicon semiconductor layer to form an alignment marking in the opening in the insulating layer. Thus, even if we accept the Examiner's erroneous assertion that the conductive poly-silicon film is a semiconductor layer, Nishihara still fails to teach or suggest, explicitly or inherently, forming an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Nishihara and request that the Examiner's rejections of claims 1-2, 4-8, and 10-12 under 35 U.S.C. 102(b) be REVERSED.

C. **Claim 3 is not obvious over Nishihara in view of Ridinger.**

As discussed above, Nishihara fails to teach or suggest providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting layer positioned above the insulating layer. Nishihara also fails to teach or suggest forming an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate. The Examiner relies on Ridinger to describe a wafer diameter. However, Ridinger fails to remedy the fundamental deficiencies of Nihihara. Accordingly, Applicants respectfully submit that the cited references fail to teach or suggest all of the claim limitations.

Moreover, the cited references also fail to provide any suggestion or motivation to modify the prior art of record to arrive at the claimed invention. To the contrary, Nishihara teaches away from the Examiner's proposed modification and combination of the cited references. In particular, Nishihara teaches that the silicon base 1 is removed to expose the alignment marking electrode 3a. See Nishihara, col. 4, ll. 27-30. Thus, Nishihara teaches away from forming an alignment marking in the silicon base 1 because the silicon base 1 will be removed.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over Nishihara and Ridinger, either alone or in combination. Applicants respectfully request that the Examiner's rejection of claim 3 under 35 U.S.C. 103(a) be REVERSED.

D. **Claim 9 is not obvious over Nishihara in view of Jang.**

As discussed above, Nishihara fails to teach or suggest providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting

layer positioned above the insulating layer. Nishihara also fails to teach or suggest forming an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate. The Examiner relies on Jang to describe use of a photolithography stepper tool. However, Jang fails to remedy the fundamental deficiencies of Nihihara. Accordingly, Applicants respectfully submit that the cited references fail to teach or suggest all of the claim limitations.

Moreover, the cited references also fail to provide any suggestion or motivation to modify the prior art of record to arrive at the claimed invention. To the contrary, Nishihara teaches away from the Examiner's proposed modification and combination of the cited references. In particular, Nishihara teaches that the silicon base 1 is removed to expose the alignment marking electrode 3a. See Nishihara, col. 4, ll. 27-30. Thus, Nishihara teaches away from forming an alignment marking in the silicon base 1 because the silicon base 1 will be removed.

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over Nishihara and Jang, either alone or in combination. Applicants respectfully request that the Examiner's rejection of claim and 9 under 35 U.S.C. 103(a) be REVERSED.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1-12 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

There is no separate Evidence Appendix for this appeal.

X. RELATED PROCEEDINGS APPENDIX

There is no Related Proceedings Appendix for this appeal.

XI. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-12, over the prior art of record. The undersigned may be contacted at (713) 934-4052 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

Date: 11/18/05

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AGENT FOR APPLICANTS

CLAIMS APPENDIX

1. (Original) A method comprising:

providing a wafer comprised of a bulk substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer positioned above said insulating layer;

forming an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate;

forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate; and

forming a layer of material above said alignment mark and in said opening.

2. (Previously Presented) The method of claim 1, wherein providing a wafer comprised of a bulk substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer positioned above said insulating layer comprises providing a wafer comprised of a bulk substrate comprised of at least one of silicon, silicon nitride, gallium arsenide, and silicon germanium.

3. (Original) The method of claim 1, wherein providing a wafer comprises providing a wafer having a diameter of at least one of approximately 4 inches, 8 inches and 12 inches.

4. (Original) The method of claim 1, wherein forming an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk

substrate comprises performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate.

5. (Original) The method of claim 1, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises:

forming a patterned layer of photoresist above said exposed surface area of said bulk substrate; and

performing at least one etching process to form said alignment mark in said exposed surface area of said bulk substrate using said patterned layer of photoresist as a mask.

6. (Original) The method of claim 1, wherein forming a layer of material above said alignment mark and in said opening comprises depositing a layer of material above said alignment mark and in said opening.

7. (Original) The method of claim 1, wherein forming a layer of material above said alignment mark and in said opening comprises forming a layer of material comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than approximately 8.0 above said alignment mark and in said opening.

8. (Original) The method of claim 1, further comprising performing a planarization operation after forming said material above said alignment mark and in said opening.

9. (Original) The method of claim 1, further comprising:

positioning said wafer in a photolithography stepper tool; and

reflecting a light off of said alignment mark formed in said bulk substrate to properly position said wafer for processing in said photolithography stepper tool.

10. (Original) The method of claim 1, wherein forming an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate comprises forming a plurality of openings in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate within each of said openings.

11. (Original) The method of claim 10, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate in each of said openings.

12. (Original) The method of claim 1, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark comprised of a plurality of grating structures in said bulk substrate within said exposed surface area of said bulk substrate.

13. (Withdrawn) A method comprising:

providing a wafer comprised of a bulk silicon substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer comprised of silicon positioned above said insulating layer;

performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate;

forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate; and

forming a layer of material above said alignment mark and in said opening.

14. (Withdrawn) The method of claim 13, wherein providing a wafer comprises providing a wafer having a diameter of at least one of approximately 4 inches, 8 inches and 12 inches.

15. (Withdrawn) The method of claim 13, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises:

forming a patterned layer of photoresist above said exposed surface area of said bulk substrate; and

performing at least one etching process to form said alignment mark in said exposed surface area of said bulk substrate using said patterned layer of photoresist as a mask.

16. (Withdrawn) The method of claim 13, wherein forming a layer of material above said alignment mark and in said opening comprises depositing a layer of material above said alignment mark and in said opening.

17. (Withdrawn) The method of claim 13, wherein forming a layer of material above said alignment mark and in said opening comprises forming a layer of material comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than approximately 8.0 above said alignment mark and in said opening.

18. (Withdrawn) The method of claim 13, further comprising performing a planarization operation after forming said material above said alignment mark and in said opening.

19. (Withdrawn) The method of claim 13, further comprising:

positioning said wafer in a photolithography stepper tool; and

reflecting a light off of said alignment mark formed in said bulk substrate to properly position said wafer for processing in said photolithography stepper tool.

20. (Withdrawn) The method of claim 13, wherein performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate comprises performing at least one etching process to form a plurality of openings in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate within each of said openings.

21. (Withdrawn) The method of claim 20, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate in each of said openings.

22. (Withdrawn) The method of claim 13, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark comprised of a plurality of grating structures in said bulk substrate within said exposed surface area of said bulk substrate.

23. (Withdrawn) A method comprising:

providing a wafer comprised of a bulk silicon substrate, an insulating layer comprised of a material having a dielectric constant less than approximately 8.0 positioned above said bulk substrate, and a semiconducting layer comprised of silicon positioned above said insulating layer;

performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate;

forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate; and

depositing a layer of material above said alignment mark and in said opening.

24. (Withdrawn) The method of claim 23, wherein providing a wafer comprises providing a wafer having a diameter of at least one of approximately 4 inches, 8 inches and 12 inches.

25. (Withdrawn) The method of claim 23, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises:

forming a patterned layer of photoresist above said exposed surface area of said bulk substrate; and

performing at least one etching process to form said alignment mark in said exposed surface area of said bulk substrate using said patterned layer of photoresist as a mask.

26. (Withdrawn) The method of claim 23, wherein depositing a layer of material above said alignment mark and in said opening comprises depositing a layer of material comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than approximately 8.0 above said alignment mark and in said opening.

27. (Withdrawn) The method of claim 23, further comprising performing a planarization operation after depositing said material above said alignment mark and in said opening.

28. (Withdrawn) The method of claim 23, further comprising:

positioning said wafer in a photolithography stepper tool; and

reflecting a light off of said alignment mark formed in said bulk substrate to properly position said wafer for processing in said photolithography stepper tool.

29. (Withdrawn) The method of claim 23, wherein performing at least one etching process to form an opening in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate comprises performing at least one etching process to form a plurality of openings in said semiconducting layer and said insulating layer to thereby expose a surface area of said bulk substrate within each of said openings.

30. (Withdrawn) The method of claim 29, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate in each of said openings.

31. (Withdrawn) The method of claim 23, wherein forming an alignment mark in said bulk substrate within said exposed surface area of said bulk substrate comprises forming an alignment mark comprised of a plurality of grating structures in said bulk substrate within said exposed surface area of said bulk substrate.

32. (Withdrawn) A wafer, comprising:

a bulk substrate;

an insulating layer positioned above said bulk substrate;

a semiconducting layer positioned above said insulating layer;

an opening formed in said semiconducting layer and said insulating layer;

an alignment mark formed in said bulk substrate within an area defined by said opening; and

a layer of material positioned above said alignment mark and within said opening.

33. (Withdrawn) The wafer of claim 32, wherein said bulk substrate comprised of at least one of silicon, silicon nitride, gallium arsenide and silicon germanium.

34. (Withdrawn) The wafer of claim 32, wherein said insulating material is comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than 8.0.

35. (Withdrawn) The wafer of claim 32, wherein said semiconducting layer is comprised of at lest one of silicon, gallium arsenide and silicon germanium.

36. (Withdrawn) The wafer of claim 32, wherein said bulk substrate is comprised of silicon and wherein said semiconducting layer is comprised of silicon.

37. (Withdrawn) The wafer of claim 32, wherein said opening is formed by performing at least one etching process.

38. (Withdrawn) The wafer of claim 32, wherein said alignment mark is comprised of a plurality of grating structures.

39. (Withdrawn) The wafer of claim 32, wherein said layer of material positioned above said alignment mark and within said opening is comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than 8.0.

40. (Withdrawn) A wafer, comprising:

a bulk substrate comprised of silicon;

an insulating layer comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than 8.0 positioned above said bulk substrate;

a semiconducting layer comprised of silicon positioned above said insulating layer;

an opening formed in said semiconducting layer and said insulating layer;

an alignment mark formed in said bulk substrate within an area defined by said opening; and

a layer of material positioned above said alignment mark and within said opening.

41. (Withdrawn) The wafer of claim 40, wherein said opening is formed by performing at least one etching process.

42. (Withdrawn) The wafer of claim 40, wherein said alignment mark is comprised of a plurality of grating structures.

43. (Withdrawn) The wafer of claim 40, wherein said layer of material positioned above said alignment mark and within said opening is comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than 8.0.

44. (Withdrawn) The method of claim 1, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon positioned above said insulating layer.

45. (Withdrawn) The method of claim 1, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of gallium arsenide positioned above said insulating layer.

46. (Withdrawn) The method of claim 1, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon germanium positioned above said insulating layer.

47. (Withdrawn) A method comprising:

providing a wafer comprised of a bulk substrate, an insulating layer positioned above said bulk substrate, and a semiconducting layer positioned above said insulating layer;

forming an opening in said semiconducting layer and said insulating layer to thereby expose an unpatterned surface area of said bulk substrate;

forming an alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate; and

forming a layer of material above said alignment mark and in said opening.

48. (Withdrawn) The method of claim 47, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon positioned above said insulating layer.

49. (Withdrawn) The method of claim 47, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of gallium arsenide positioned above said insulating layer.

50. (Withdrawn) The method of claim 47, wherein providing the wafer comprised of the bulk substrate, the insulating layer positioned above said bulk substrate, and the semiconducting layer positioned above said insulating layer comprises providing a semiconducting layer comprised of silicon germanium positioned above said insulating layer.

51. (Withdrawn) The method of claim 47, wherein forming the opening in said semiconducting layer and said insulating layer to thereby expose the unpatterned surface area of

said bulk substrate comprises performing at least one etching process to form the opening in said semiconducting layer and said insulating layer to thereby expose the unpatterned surface area of said bulk substrate.

52. (Withdrawn) The method of claim 47, wherein forming the alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate comprises:

forming a patterned layer of photoresist above said exposed unpatterned surface area of said bulk substrate; and

performing at least one etching process to form said alignment mark in said exposed unpatterned surface area of said bulk substrate using said patterned layer of photoresist as a mask.

53. (Withdrawn) The method of claim 47, wherein forming the layer of material above said alignment mark and in said opening comprises depositing a layer of material above said alignment mark and in said opening.

54. (Withdrawn) The method of claim 47, wherein forming the layer of material above said alignment mark and in said opening comprises forming a layer of material comprised of at least one of silicon dioxide, silicon oxynitride, silicon nitride and a material having a dielectric constant less than approximately 8.0 above said alignment mark and in said opening.

55. (Withdrawn) The method of claim 47, further comprising performing a planarization operation after forming said material above said alignment mark and in said opening.

56. (Withdrawn) The method of claim 47, further comprising:

positioning said wafer in a photolithography stepper tool; and

reflecting a light off of said alignment mark formed in said bulk substrate to properly position said wafer for processing in said photolithography stepper tool.

57. (Withdrawn) The method of claim 47, wherein forming the opening in said semiconducting layer and said insulating layer to thereby expose the unpatterned surface area of said bulk substrate comprises forming a plurality of openings in said semiconducting layer and said insulating layer to thereby expose an unpatterned surface area of said bulk substrate within each of said openings.

58. (Withdrawn) The method of claim 57, wherein forming the alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate comprises forming an alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate in each of said openings.

59. (Withdrawn) The method of claim 47, wherein forming the alignment mark in said bulk substrate within said exposed unpatterned surface area of said bulk substrate comprises

forming an alignment mark comprised of a plurality of grating structures in said bulk substrate within said exposed unpatterned surface area of said bulk substrate.